Specifications for the NI PXI-5421

16-Bit 100 MS/s Arbitrary Waveform Generator

Contents

Unless otherwise noted, the following conditions were used for each specification:

- Analog Filter enabled.
- Interpolation set to maximum allowed factor for a given sample rate.
- Signals terminated with 50 Ω.
- Direct Path set to 1 V_{pk-pk}, Low-Gain Amplifier Path set to 2 V_{pk-pk}, and High-Gain Amplifier Path set to 12 V_{pk-pk}.
- Sample clock set to 100 MS/s.

Specifications are subject to change without notice.

NATIONAL INSTRUMENTS™

CH 0 (Channel 0 Analog Output, Front Panel Connector)

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td>Number of Channels</td><td colspan="4">One</td><td>—</td></tr>
<tr><td>Connector</td><td colspan="4">SMB (jack)</td><td>—</td></tr>
<tr><td colspan="6">Output Voltage Characteristics</td></tr>
<tr><td>Output Paths</td><td colspan="4">1. The software-selectable Main Output Path setting provides full-scale voltages from 12.00 V_{pk-pk} to 5.64 mV_{pk-pk} into a 50 Ω load. NI-FGEN uses either the Low-Gain Amplifier or the High-Gain Amplifier when the Main Output Path is selected, depending on the Gain attribute.
2. The software-selectable Direct Path is optimized for IF applications and provides full-scale voltages from 1.000 V_{pk-pk} to 0.707 V_{pk-pk}.</td><td>—</td></tr>
<tr><td>DAC Resolution</td><td colspan="4">16 bits</td><td>—</td></tr>
<tr><td>Amplitude Resolution</td><td colspan="4">3 digits</td><td>—</td></tr>
<tr><td colspan="6">Amplitude and Offset</td></tr>
<tr><td rowspan="10">Amplitude Range</td><td rowspan="2">Path</td><td rowspan="2">Load</td><td colspan="2">Amplitude (V_{pk-pk})</td><td rowspan="10">1. Amplitude values assume the full scale of the DAC is utilized. If an amplitude smaller than the minimum value is desired, then waveforms less than full scale of the DAC can be used.
2. Driver software compensates for user-specified resistive loads.</td></tr>
<tr><td>Minimum Value</td><td>Maximum Value</td></tr>
<tr><td rowspan="3">Direct</td><td>50 Ω</td><td>0.707</td><td>1.000</td></tr>
<tr><td>1 kΩ</td><td>1.347</td><td>1.905</td></tr>
<tr><td>Open</td><td>1.414</td><td>2.000</td></tr>
<tr><td rowspan="3">Low-Gain Amplifier</td><td>50 Ω</td><td>0.00564</td><td>2.000</td></tr>
<tr><td>1 kΩ</td><td>0.01073</td><td>3.810</td></tr>
<tr><td>Open</td><td>0.01127</td><td>4.000</td></tr>
<tr><td rowspan="3">High-Gain Amplifier</td><td>50 Ω</td><td>0.0338</td><td>12.00</td></tr>
<tr><td>1 kΩ</td><td>0.06441</td><td>22.86</td></tr>
<tr><td>Open</td><td>0.06763</td><td>24.00</td></tr>
</table>

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>Offset Range</td><td colspan="3">Span of ±25% of Amplitude range with increments <0.0014% of Amplitude range.</td><td>Not available on the Direct Path.</td></tr>
<tr><td colspan="5">Maximum Output Voltage</td></tr>
<tr><td rowspan="10">Maximum Output Voltage</td><td>Path</td><td>Load</td><td>Maximum Output Voltage (V_{pk-pk})</td><td rowspan="10">The Maximum Output Voltage of the NI 5421 is determined by the Amplitude Range and the Offset Range.</td></tr>
<tr><td rowspan="3">Direct</td><td>50 Ω</td><td>±0.500</td></tr>
<tr><td>1 kΩ</td><td>±0.953</td></tr>
<tr><td>Open</td><td>±1.000</td></tr>
<tr><td rowspan="3">Low-Gain Amplifier</td><td>50 Ω</td><td>±1.000</td></tr>
<tr><td>1 kΩ</td><td>±1.905</td></tr>
<tr><td>Open</td><td>±2.000</td></tr>
<tr><td rowspan="3">High-Gain Amplifier</td><td>50 Ω</td><td>±6.000</td></tr>
<tr><td>1 kΩ</td><td>±11.43</td></tr>
<tr><td>Open</td><td>±12.00</td></tr>
<tr><td colspan="5">Accuracy</td></tr>
<tr><td rowspan="2">DC Accuracy</td><td colspan="3">For the Low-Gain or High-Gain Amplifier Path:
± 0.2% of Amplitude ± 0.05% of Offset ± 500 µV (within ±10 °C of self-calibration temperature)
± 0.4% of Amplitude ± 0.05% of Offset ± 1 mV (0 °C to 55 °C)</td><td rowspan="2">All paths are calibrated for amplitude and gain errors. The Low-Gain and High-Gain Amplifier Paths are also calibrated for offset errors.</td></tr>
<tr><td colspan="3">For the Direct Path:
Gain Accuracy: ±0.2% (within ±10 °C of self-calibration temperature)
Gain Accuracy: ±0.4% (0 °C to 55 °C)
DC Error: ±30 mV (0 °C to 55 °C)</td></tr>
<tr><td>AC Amplitude Accuracy</td><td colspan="3">± 1.0% of Amplitude ± 1 mV</td><td>50 kHz sine wave</td></tr>
<tr><td colspan="5">Output Characteristics</td></tr>
<tr><td>Output Impedance</td><td colspan="3">50 Ω or 75 Ω, software selectable.</td><td>—</td></tr>
<tr><td>Load Impedance Compensation</td><td colspan="3">Output amplitude is compensated for user-specified load impedances.</td><td>—</td></tr>
</table>

Specification	Value			Comments
Output Coupling	DC			—
Output Enable	Software selectable. When disabled, CH 0 out is pulled low with a 1 W resistor with a value equal to the selected output impedance.			—
Maximum Output Overload	The CH 0 output can be connected to a 50 Ω, ±12 V (±8 V for the Direct Path) source without sustaining any damage. No damage occurs if the CH 0 output is shorted to ground indefinitely.			—
Waveform Summing	The CH 0 output supports waveform summing among similar paths—specifically, the outputs of multiple NI-5421 modules can be connected together.			—
Frequency and Transient Response				
Bandwidth	43 MHz			Measured at –3 dB.
Digital Interpolation Filter	Software-selectable Finite Impulse Response (FIR) filter. Available interpolation factors are 2, 4, or 8.			—
Analog Filter	Seven-pole elliptical filter.			—
Passband Flatness	Path			—
	Direct	Low-Gain and High-Gain Amplifier		
	±0.25 dB 100 Hz to 40 MHz	+0.5 dB to –1.0 dB 100 Hz to 20 MHz		
Pulse Response	Path			Analog Filter and Digital Interpolation Filter disabled.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
Rise/Fall Time	<5 ns	<8 ns	<10 ns	
Aberration	<10 %	<5 %	<5 %	

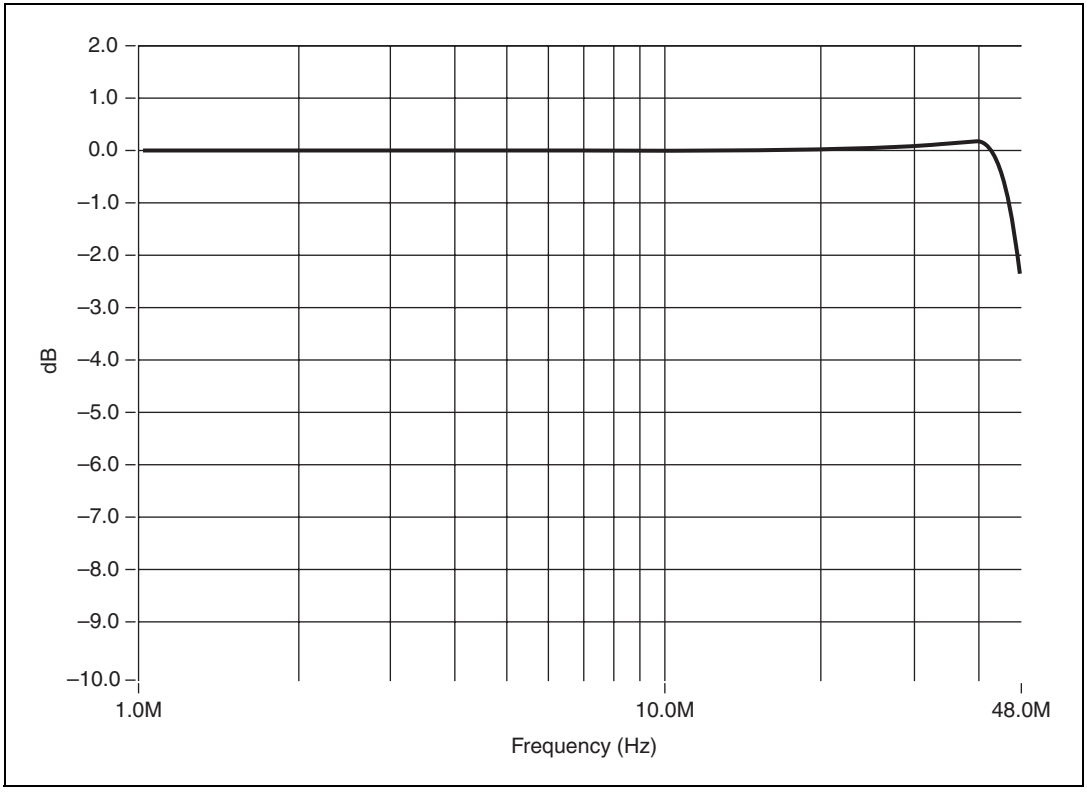

Figure 1. Normalized Passband Flatness, Direct Path

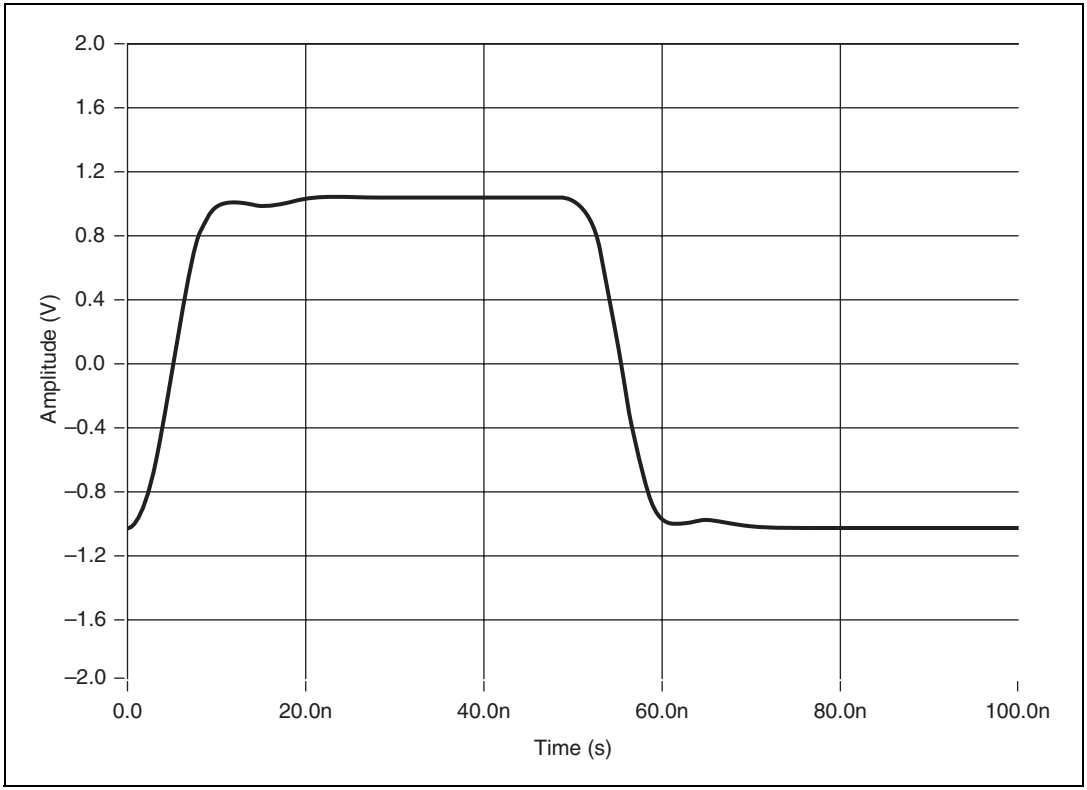

Figure 2. Pulse Response, Low-Gain Path, 50 Ω Load

Specification	Value			Comments
Suggested Maximum Frequencies for Common Functions				
Function	Path			Disable the Analog Filter and the Digital Interpolation Filter for square, ramp, and triangle.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
Sine	43 MHz	43 MHz	43 MHz	
Square	Not Recommended	25 MHz	12.5 MHz	
Ramp	Not Recommended	5 MHz	5 MHz	
Triangle	Not Recommended	5 MHz	5 MHz	

Specification	Value			Comments
Spectral Characteristics				
Signal to Noise and Distortion (SINAD)	Path			Amplitude –1 dBFS. Measured from DC to 50 MHz. SINAD at low amplitudes is limited by a –148 dBm/Hz noise floor.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	64 dB	66 dB	63 dB	
5 MHz	63 dB	64 dB	59 dB	
10 MHz	61 dB	60 dB	47 dB	
20 MHz	57 dB	56 dB	42 dB	
30 MHz	60 dB	62 dB	62 dB	
40 MHz	60 dB	62 dB	62 dB	
43 MHz	58 dB	60 dB	55 dB	
Spurious Free Dynamic Range with Harmonics	Path			Amplitude –1 dBFS. Measured from DC to 50 MHz. Also called harmonic distortion. SFDR with harmonics at low amplitudes is limited by a –148 dBm/Hz noise floor.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	–76 dBc	–71 dBc	–58 dBc	
5 MHz	–73 dBc	–68 dBc	–55 dBc	
10 MHz	–68 dBc	–64 dBc	–47 dBc	
20 MHz	–60 dBc	–57 dBc	–42 dBc	
30 MHz	–73 dBc	–73 dBc	–74 dBc	
40 MHz	–76 dBc	–73 dBc	–74 dBc	
43 MHz	–78 dBc	–75 dBc	–59 dBc	

Specification	Value			Comments
Spurious Free Dynamic Range without Harmonics	Path			Amplitude –1 dBFS. Measured from DC to 50 MHz. SFDR without harmonics at low amplitudes is limited by a –148 dBm/Hz noise floor.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	–88 dBFS	–91 dBFS	–91 dBFS	
5 MHz	–88 dBFS	–91 dBFS	–91 dBFS	
10 MHz	–87 dBFS	–89 dBFS	–91 dBFS	
20 MHz	–80 dBFS	–89 dBFS	–89 dBFS	
30 MHz	–73 dBFS	–73 dBFS	–74 dBFS	
40 MHz	–76 dBFS	–73 dBFS	–74 dBFS	
43 MHz	–78 dBFS	–75 dBFS	–60 dBFS	
Total Harmonic Distortion (THD)	Path			Amplitude –1 dBFS. Includes the 2nd through the 6th harmonic. For 0 °C to 40 °C, the 40 MHz and 43 MHz values for the low-gain amplifier and high-gain amplifier improve to –50 dBc and –32 dBc respectively.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
20 kHz	–77 dBc (0.014%)	–77 dBc (0.014%)	–77 dBc (0.014%)	
1 MHz	–75 dBc	–70 dBc	–62 dBc	
5 MHz	–69 dBc	–65 dBc	–54 dBc	
10 MHz	–67 dBc	–62 dBc	–47 dBc	
20 MHz	–60 dBc	–54 dBc	–42 dBc	
30 MHz	–54 dBc	–50 dBc	–39 dBc	
40 MHz	–50 dBc	–45 dBc	–30 dBc	
43 MHz	–50 dBc	–45 dBc	–30 dBc	

Specification	Value			Comments
Intermodulation Distortion (IMD)	Path			Each tone is –7 dBFS.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
10.2 MHz and 11.2 MHz	–90 dBc	–79 dBc	–59 dBc	
10.6 MHz and 10.8 MHz	–89 dBc	–79 dBc	–59 dBc	
19.5 MHz and 20.5 MHz	–83 dBc	–69 dBc	–52 dBc	
19.9 MHz and 20.1 MHz	–85 dBc	–69 dBc	–52 dBc	
34.0MHz and 35.0 MHz	–81 dBc	–59 dBc	–51 dBc	
34.8 MHz and 35.0 MHz	–79 dBc	–57 dBc	–50 dBc	
42.0 MHz and 43.0 MHz	–85 dBc	–56 dBc	–51 dBc	
42.8 MHz and 43.0 MHz	–81 dBc	–54 dBc	–50 dBc	

Specification	Value					Comments
Average Noise Density		Amplitude Range		Average Noise Density			Average Noise Density at small amplitudes is limited by a –148 dBm/Hz Noise Floor.
	Path	V_{pk-pk}	dBm	nV/Hz	dBm/Hz	dBFS/Hz	
	Direct	1	4.0	18	–142	–146.0	
	Low Gain	0.06	–20.4	9	–148	–127.6	
	Low Gain	0.1	–16.0	9	–148	–132.0	
	Low Gain	0.4	–4.0	13	–145	–141.0	
	Low Gain	1	4.0	18	–142	–146.0	
	Low Gain	2	10.0	35	–136	–146.0	
	High Gain	4	16.0	71	–130	–146.0	
	High Gain	12	25.6	213	–120	–145.6	

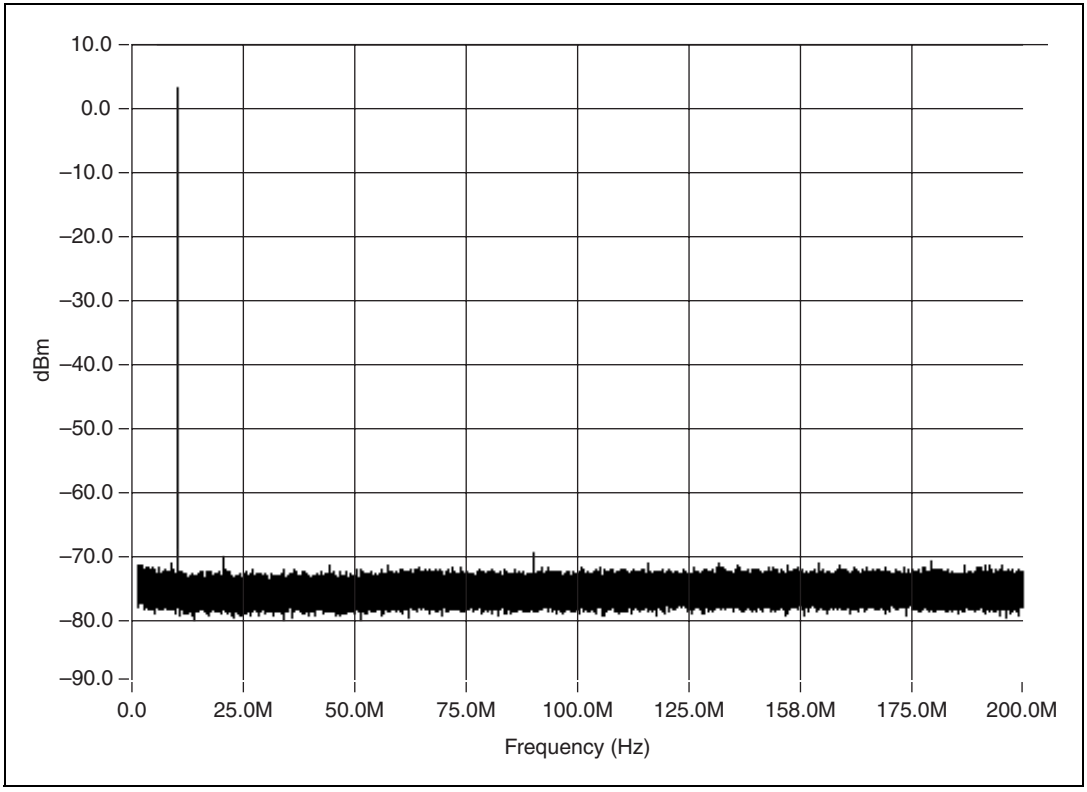

Figure 3. 10 MHz Single-Tone Spectrum, Direct Path, 100 MS/s, Interpolation Factor Set to 4.

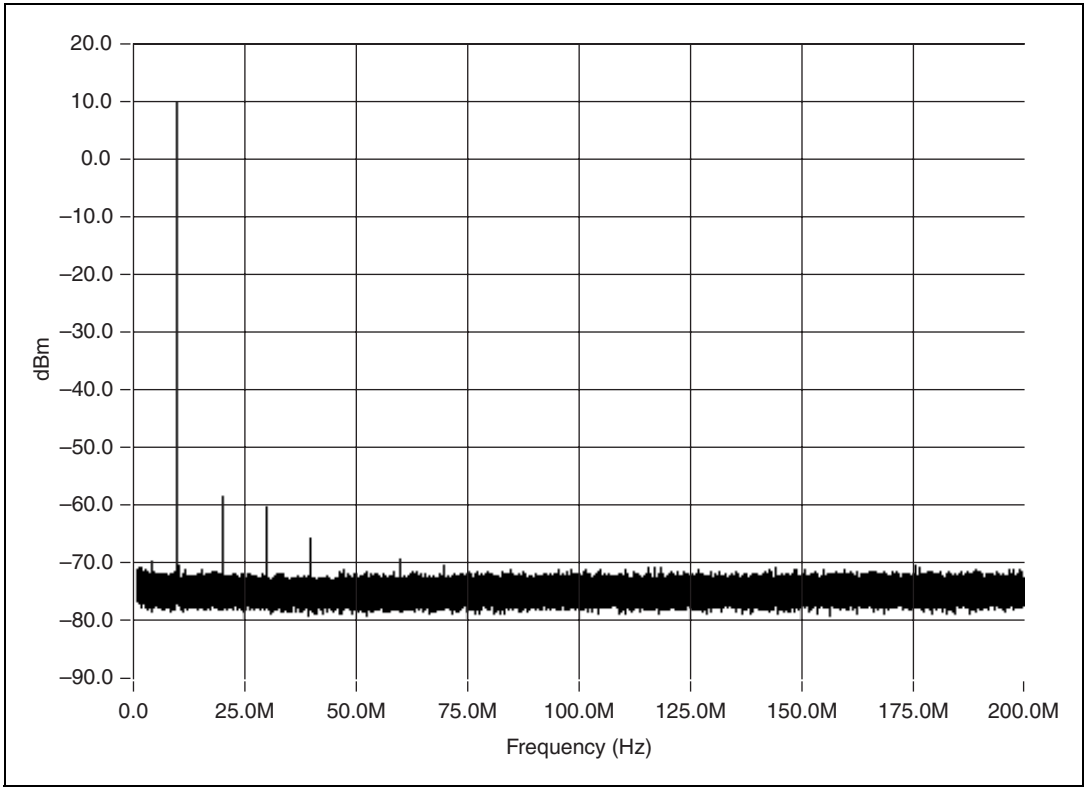

Figure 4. 10 MHz Single-Tone Spectrum, Low-Gain Amplifier Path, 100 MS/s, Interpolation Factor Set to 4.

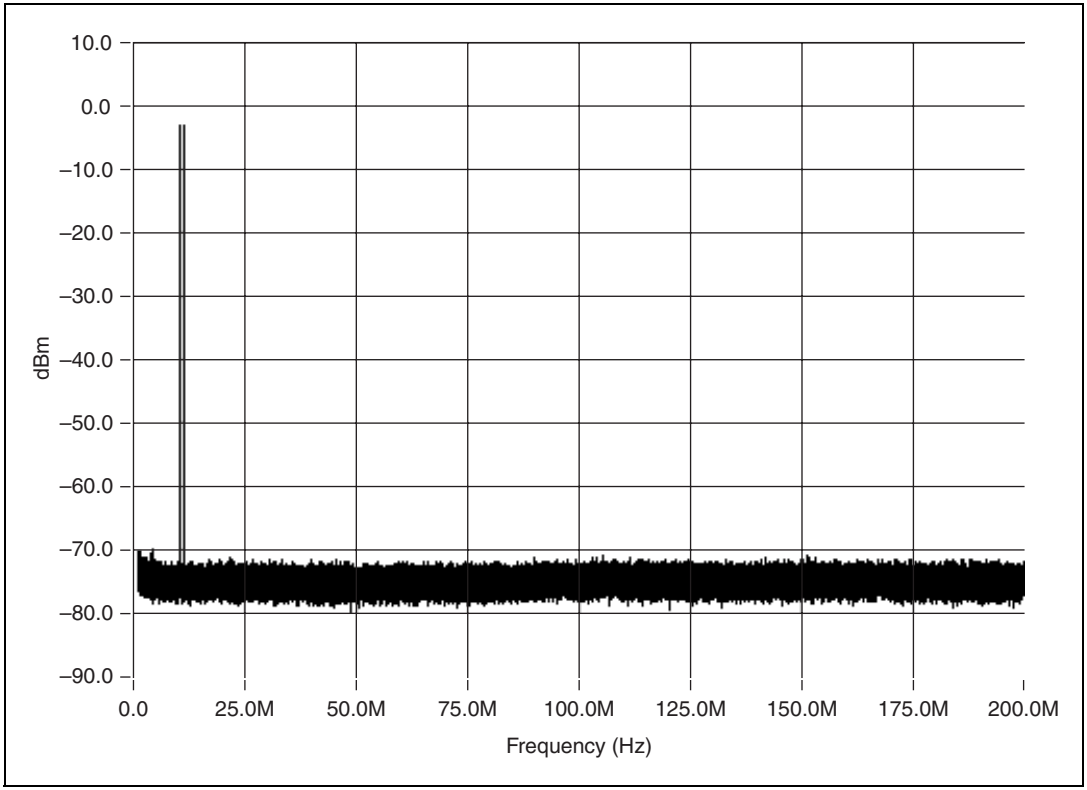

Figure 5. Direct Path, 2-Tone Spectrum

Sample Clock

Specification	Value	Comments
Sources	1. Internal, Divide-by-N (N ≥ 1) 2. Internal, DDS-based, High-Resolution 3. External, CLK IN (SMB front panel connector) 4. External, DDC Clk In (DIGITAL DATA & CONTROL front panel connector) 5. External, PXI Star trigger (backplane connector) 6. External, PXI_TRIG <0..7> (backplane connector)	Refer to the *Onboard Clock (Internal VCXO)* section for more information about Internal Clock Sources.

Specification	Value			Comments
Sample Rate Range and Resolution				
Sample Clock Source	Sample Rate Range		Sample Rate Resolution	—
Divide-by-N	23.84 S/s to 100 MS/s		Settable to (100 MS/s) / N 1 ≤ N ≤ 4,194,304	
High Resolution	10 S/s to 100 MS/s		1.06 µHz	
CLK IN	200 kS/s to 105 MS/s		Resolution determined by external source. External Sample Clock duty cycle tolerance 40% to 60%.	
DDC Clk In	10 S/s to 105 MS/s			
PXI Star Trigger	10 S/s to 105 MS/s			
PXI_TRIG <0:7>	10 S/s to 20 MS/s			
Effective Sample Rate				
	Sample Rate (MS/s)	Interpolation Factor	Effective Sample Rate	Effective Sample Rate = (Interpolation Factor) * (Sample Rate)
	10 S/s to 105 MS/s	1 (Off)	10 S/s to 105 MS/s	
	12.5 MS/s to 105 MS/s	2	25 MS/s to 210 MS/s	
	10 MS/s to 100 MS/s	4	40 MS/s to 400 MS/s	
	10 MS/s to 50 MS/s	8	80 MS/s to 400 MS/s	
Sample Clock Delay Range and Resolution				
Sample Clock Source	Delay Adjustment Range		Delay Adjustment Resolution	—
Divide-by-N	±1 sample clock period		<21 ps	
High Resolution	±1 sample clock period		Sample Clock Period/16,384	
External (all)	0 ns to 7.6 ns		<15 ps	

Specification	Value				Comments
System Phase Noise and Jitter (10 MHz Carrier)					
Sample Clock Source	System Phase Noise Density (dBc/Hz) Offset			System Output Jitter (Integrated from 100 Hz to 100 kHz)	1. High-Resolution specifications increase as the sample rate is decreased. 2. PXI Star trigger specification valid when sample clock source is locked to PXI_CLK10.
	100 Hz	1 kHz	10 kHz		
Divide-by-N	–110	–131	–137	<1.0 ps rms	
High Resolution	–114	–126	–126	<4.0 ps rms	
CLK IN	–113	–132	–135	<1.1 ps rms	
PXI Star Trigger	–115	–118	–130	<3.0 ps rms	
External Sample Clock Input Jitter Tolerance	Cycle-Cycle Jitter ±300 ps Period Jitter ±1 ns				—
Sample Clock Exporting					
Exported Sample Clock Destinations	1. PFI<0..1> (SMB front panel connectors) 2. DDC Clk Out (DIGITAL DATA & CONTROL front panel connector) 3. PXI_TRIG<0..7> (backplane connector)				Exported Sample Clocks can be divided by integer K ($1 \le K \le 4{,}194{,}304$)
Exported Sample Clock Destinations	Maximum Frequency		Jitter (Typical)	Duty Cycle	—
PFI<0..1>	105 MHz		PFI0: 6 ps rms PFI1: 12 ps rms	25% to 60%	
DDC Clk Out	105 MHz		40 ps rms	40% to 60%	
PXI_TRIG <0..7>	20 MHz		—	—	

Onboard Clock (Internal VCXO)

Specification	Value	Comments
Clock Source	Internal sample clocks can either be locked to a Reference Clock using a phase-locked loop or be derived from the onboard VCXO frequency reference.	—
Frequency Accuracy	±25 ppm	—

Phase-Locked Loop (PLL) Reference Clock

Specification	Value	Comments
Sources	1. PXI_CLK10 (backplane connector) 2. CLK IN (SMB front panel connector)	The PLL Reference Clock provides the reference frequency for the phase-locked loop.
Frequency Accuracy	When using the PLL, the Frequency Accuracy of the NI 5421 is solely dependent on the Frequency Accuracy of the PLL Reference Source.	—
Lock Time	Typical: 70 ms. Maximum: 200 ms.	—
Frequency Range	5 MHz to 20 MHz in increments of 1 MHz. Default of 10 MHz. The PLL Reference Clock Frequency has to be accurate to ±50 ppm.	—
Duty Cycle Range	40% to 60%	—
Exported PLL Reference Clock Destinations	1. PFI<0..1> (SMB front panel connectors) 2. PXI_Trig<0..7> (backplane connector)	—

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Specification	Value	Comments
Connector	SMB (jack)	—
Direction	Input	—
Destinations	1. Sample Clock 2. PLL Reference Clock	—
Frequency Range	1 MHz to 105 MHz (Sample Clock destination and sine waves) 200 kHz to 105 MHz (Sample Clock destination and square waves) 5 MHz to 20 MHz (PLL Reference Clock destination)	—
Input Voltage Range	Sine wave: 0.65 V_{pk-pk} to 2.8 V_{pk-pk} (0 dBm to +13 dBm) Square wave: 0.2 V_{pk-pk} to 2.8 V_{pk-pk}	—
Maximum Input Overload	±10 V	—
Input Impedance	50 Ω	—
Input Coupling	AC	—

PFI 0 and PFI 1 (Programmable Function Interface, Front Panel Connectors)

Specification	Value	Comments
Connectors	2 SMB (jack)	—
Direction	Bi-directional	—
Frequency Range	DC to 105 MHz	—
As an Input (Trigger)		
Destinations	Start Trigger	—
Maximum Input Overload	–2 V to +7 V	—
V_{IH}	2.0 V	—
V_{IL}	0.8 V	—
Input Impedance	1 kΩ	—
As an Output (Event)		
Sources	1. Sample Clock divided by integer K ($1 \le K \le 4{,}194{,}304$) 2. Sample Clock Timebase (100 MHz) divided by integer M ($2 \le M \le 4{,}194{,}304$) 3. PLL Reference Clock 4. Marker 5. Exported Start Trigger (Out Start Trigger)	—
Output Impedance	50 Ω	—
Maximum Output Overload	–2 V to +7 V	—
V_{OH}	Minimum: 2.9 V (open load), 1.4 V (50 Ω load)	Output drivers are +3.3 V TTL compatible.
V_{OL}	Maximum: 0.2 V (open load), 0.2 V (50 Ω load)	
Rise/Fall Time	≤2.5 ns	Load of 10 pF

Digital Data & Control, DDC (Optional Front Panel Connector)

Specification	Value			Comments
Connector Type	68-pin VHDCI female receptacle			—
Number of Data Output Signals	16			—
Control Signals (6)	DDC Clk Out (clock output)			—
	DDC Clk In (clock input)			
	PFI<2..3> (inputs)			
	PFI<4..5> (outputs)			
Ground	23 pins			—
Output Signal Characteristics (Includes Data Outputs, DDC Clk Out, and PFI <4..5>)				
Signal Type	LVDS (Low-Voltage Differential Signal)			—
Signal Characteristics	Minimum	Typical	Maximum	1. Tested with 100 Ω differential load. 2. Measured at the front panel. 3. Load capacitance <15 pF. 4. Driver and receiver comply with ANSI/TIA/EIA-644.
V_{OH}	—	1.3 V	1.7 V	
V_{OL}	0.8 V	1.0 V	—	
Differential Output Voltage	0.25 V	—	0.45 V	
Output Common-Mode Voltage	1.125 V	—	1.375 V	
Differential Pulse Skew (skew within a differential pair)	—	—	0.6 ns	
Rise/Fall Time	—	0.5 ns	1.6 ns	
Output Skew	Typical: 1 ns, maximum 2 ns. Skew between any two outputs on the DIGITAL DATA & CONTROL front panel connector.			—

Specification	Value		Comments
Output Enable/Disable	Controlled through the software on all Data Output Signals and Control Signals collectively. When disabled, the outputs go to a high-impedance state.		—
Maximum Output Overload	–0.3 V to +3.9 V		—
Input Signal Characteristics (Includes DDC Clk In and PFI <2:3>)			
Signal Type	LVDS (Low-Voltage Differential Signal)		—
Input Differential Impedance	100 Ω		—
Maximum Output Overload	–0.3 V to +3.9 V		—
Signal Characteristics	Minimum	Maximum	—
Differential Input Voltage	0.1 V	0.5 V	
Input Common Mode Voltage	0.2 V	2.2 V	
DDC Clk Out			
Clocking Format	Data outputs and markers change on the falling edge of DDC Clk Out.		—
Frequency Range	Refer to the *Sample Clock* section for more information.		—
Duty Cycle	40% to 60%		—
Jitter	40 ps rms		—
DDC Clk In			
Clocking Format	DDC Data Output signals change on the rising edge of DDC Clk In.		—
Frequency Range	10 Hz to 105 MHz		—

Specification	Value	Comments
Input Duty Cycle Tolerance	40% to 60%	—
Input Jitter Tolerances	300 ps pk-pk of Cycle-Cycle Jitter, and 1 ns rms of Period Jitter.	—

Start Trigger

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>Sources</td><td colspan="2">1. PFI<0..1> (SMB front panel connectors)
2. PFI<2..3> (DIGITAL DATA & CONTROL front panel connector)
3. PXI_TRIG<0..7> (backplane connector)
4. PXI Star trigger (backplane connector)
5. Software (use function call)
6. Immediate (does not wait for a trigger). Default.</td><td>—</td></tr>
<tr><td>Modes</td><td colspan="2">1. Single
2. Continuous
3. Stepped
4. Burst</td><td>—</td></tr>
<tr><td>Edge Detection</td><td colspan="2">Rising</td><td>—</td></tr>
<tr><td>Minimum Pulse Width</td><td colspan="2">25 ns. Refer to t_{s1} at NI Signal Generators Help»Devices» NI PXI-5421 Overview»Triggering»Trigger Timing.</td><td>—</td></tr>
<tr><td rowspan="5">Delay from Start Trigger to CH 0 Analog Output</td><td>Interpolation Factor</td><td>Typical Delay</td><td rowspan="5">Refer to t_{s2} at NI Signal Generators Help»Devices» NI PXI-5421 Overview» Triggering» Trigger Timing.</td></tr>
<tr><td>Digital Interpolation Filter disabled.</td><td>43 Sample Clock Periods + 110 ns</td></tr>
<tr><td>2</td><td>57 Sample Clock Periods + 110 ns</td></tr>
<tr><td>4</td><td>63 Sample Clock Periods + 110 ns</td></tr>
<tr><td>8</td><td>64 Sample Clock Periods + 110 ns</td></tr>
</table>

Specification	Value	Comments
Delay from Start Trigger to Digital Data Output	40 Sample Clock periods + 110 ns.	—
Trigger Exporting		
Exported Trigger Destinations	A signal used as a trigger can be routed out to any destination listed in the Marker Destination specification.	—
Exported Trigger Delay	65 ns (typical). Refer to t_{s3} at **NI Signal Generators Help» Devices»NI PXI-5421 Overview»Triggering»Trigger Timing**.	—
Exported Trigger Pulse Width	>150 ns. Refer to t_{s4} at **NI Signal Generators Help» Devices»NI PXI-5421 Overview»Triggering»Trigger Timing**.	—

Markers

Specification	Value	Comments
Destinations	1. PFI<0..1> (SMB front panel connectors) 2. PFI<4..5> (DIGITAL DATA & CONTROL front panel connector) 3. PXI_TRIG<0..7> (backplane connector)	—
Quantity	One Marker per Segment.	—
Quantum	Marker position must be placed at an integer multiple of four samples.	—
Width	>150 ns. Refer to t_{m2} at **NI Signal Generators Help» Devices»NI PXI-5421 Overview»Waveform Generation»Marker Events**.	—

Specification	Value			Comments
Skew	Destination	With Respect to Analog Output	With Respect to Digital Data Output	Refer to t_{m1} at **NI Signal Generators Help»Devices» NI PXI-5421 Overview» Waveform Generation» Marker Events**.
	PFI<0..1>	±2 Sample Clock Periods	N/A	
	PFI<4..5>	N/A	<2 ns	
	PXI_Trig<0..7>	±2 Sample Clock Periods	N/A	
Jitter	20 ps rms			—

Waveform and Instruction Memory Utilization

Specification	Value			Comments
Memory Usage	The NI 5421 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.			For more information, refer to **NI Signal Generators Help»Devices» NI PXI-5421» Onboard Memory**
Onboard Memory Size	8 MB standard: 8,388,608 bytes	32 MB option: 33,554,432 bytes	256 MB option: 268,435,456 bytes	—
Output Modes	Arbitrary Waveform mode and Arbitrary Sequence mode			—
Arbitrary Waveform Mode	In Arbitrary Waveform mode, a single waveform is selected from the set of waveforms stored in onboard memory and generated.			—
Arbitrary Sequence Mode	In Arbitrary Sequence mode, a sequence directs the NI 5421 to generate a set of waveforms in a particular order. Elements of the sequence are referred to as segments. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) the waveform is generated, and which sample in the waveform a marker output signal occurs.			—

Specification	Value			Comments
Minimum Waveform Size (Samples)		Arbitrary Waveform Mode	Arbitrary Sequence Mode	The minimum waveform size is sample rate dependent in Arbitrary Sequence Mode.
	Single Trigger Mode	16	16	
	Continuous Trigger Mode	16	96 @ > 50 MS/s	
			32 @ ≤ 50 MS/s	
	Stepped Trigger Mode	32	96 @ > 50 MS/s	
			32 @ ≤ 50 MS/s	
	Burst Trigger Mode	16	512 @ > 50 MS/s	
			256 @ ≤ 50 MS/s	
Loop Count	1 to 16,777,215. Burst trigger: Unlimited			—
Quantum	Waveform size must be an integer multiple of four samples.			—
Memory Limits				
	8 MB standard	32 MB option	256 MB option	All trigger modes except where noted.
Arbitrary Waveform Mode Maximum Waveform Memory	4,194,176 Samples	16,777,088 Samples	134,217,600 Samples	
Arbitrary Sequence Mode Maximum Waveform Memory	4,194,120 Samples	16,777,008 Samples	134,217,520 Samples	Condition: One or two segments in a sequence.

Specification	Value			Comments
Arbitrary Sequence Mode Maximum Waveforms	65,000 Burst trigger: 8,000	262,000 Burst trigger: 32,000	2,097,000 Burst trigger: 262,000	Condition: One or two segments in a sequence.
Arbitrary Sequence Mode Maximum Segments in a Sequence	104,000 Burst trigger: 65,000	418,000 Burst trigger: 262,000	3,354,000 Burst trigger: 2,090,000	Condition: Waveform memory is <4,000 samples.

Calibration

Specification	Value	Comments
Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 75 seconds to complete.	—
External Calibration	The External Calibration calibrates the VCXO, voltage reference, output impedance, DC gain, and offset. Appropriate constants are stored in non volatile memory.	—
Calibration Interval	Specifications valid within 2 years of External Calibration.	—
Warm-up Time	15 minutes	—

Power

Specification	Typical Operation	Overload Operation	Comments
+3.3 VDC	1.9 A	2.7 A	Typical. Overload operation occurs when CH 0 is shorted to ground.
+5 VDC	2.0 A	2.2 A	
+12 VDC	0.46 A	0.5 A	
–12 VDC	0.01 A	0.01 A	
Total Power	21.9 W	26.0 W	

Software

Specification	Value	Comments
Driver Software	NI-FGEN 2.0 or later version. NI-FGEN is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5421. NI-FGEN provides application programming interfaces for many development environments.	—
Application Software	NI-FGEN provides programming interfaces for the following application development environments: • LabVIEW • LabWindows™/CVI™ • Measurement Studio • Microsoft Visual C++ • Microsoft Visual C/C++ • Microsoft Visual Basic • Borland C/C++	—
Soft Front Panel/ Interactive Configuration	The FGEN Soft Front Panel 1.3 or later supports interactive control of the NI 5421. The FGEN Soft Front Panel is included on the NI-FGEN driver CD. Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the NI 5421. MAX is also included on the NI-FGEN CD.	—

Environment

Specifications	Value	Comments
Operating Temperature	0 ºC to +55 ºC in all NI PXI chassis except the following. 0 ºC to +45 ºC when installed in an NI PXI-101*x* or PXI-1000B chassis.	—
Storage Temperature	–25 ºC to +85 ºC	—
Operating Relative Humidity	10% to 90%, noncondensing	—
Storage Relative Humidity	5% to 95%, noncondensing	—
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Operating Vibration	5 Hz to 500 Hz, 0.31 g_{rms}. Meets IEC-60068-2-64.	—
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms}. Meets IEC-60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	0 m to 2000 m above sea level	—
Pollution Degree	2	—

Safety, Electromagnetic Compatibility, and CE Compliance

Specification	Value	Comments
Safety	The NI 5421 meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use: IEC 61010-1, EN 61010-1 UL 3111-1, UL 61010B-1 CAN/CSA C22.2 No. 1010.1	For UL and other safety certifications, refer to the product label or to `ni.com`.
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	—
Immunity	EN 61326:1997 + A2:2001, Table 1	—
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant For EMC compliance, you must operate this device with shielded cabling.	—
This product meets the essential requirements of applicable European Directives, as amended for CE Marking, as follows:		
Low-Voltage Directive (safety)	73/23/EEC	—
Electromagnetic Compatibility Directive (EMC)	89/336/EEC	—
Note: Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declarations of Conformity Information** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.		

Physical

Specification	Value		Comments
Dimensions	Single 3U PXI slot. Also CompactPCI compatible.		—
Front Panel Connectors			
Label	Function(s)	Connector Type	—
CH0	Analog Output	SMB (jack)	
CLK IN	Sample clock input and PLL reference clock input.	SMB (jack)	
PFI 0	Marker output, trigger input, sample clock output, exported trigger output and PLL reference clock output.	SMB (jack)	
PFI 1	Marker output, trigger input, sample clock output, exported trigger output and PLL reference clock output.	SMB (jack)	
DIGITAL DATA & CONTROL	Digital data output, trigger input, exported trigger output, markers, external sample clock input, and sample clock output.	68-pin VHDCI Female Receptacle	
Front Panel Indicators			
	Access LED	Active LED	For more information, refer to **NI Signal Generators Help»Devices» NI PXI-5421 Overview» Front Panel Connectors» Access and Active LEDs**
	The Access LED indicates the status of the PCI bus and the interface from the NI 5421 to the controller.	The Active LED indicates the status of the onboard generation hardware of the NI 5421.	
Included Cable			
	One (NI part number 763541-01), 50 Ω, BNC Male to SMB Plug, RG223/U, Double Shielded, 1 meter cable.		—

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